

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listing, of claims in the application:

**Listing of Claims:**

1. (currently amended) A semiconductor FinFET device comprising:
  - an insulator;
  - a semiconductor layer formed on the insulator, the semiconductor layer including a fin portion corresponding to a channel of the semiconductor device;
  - a source region formed at a first end of the semiconductor layer, a height of the source region being higher than that of the fin;
  - a drain region formed at a second end of the semiconductor layer, a height of the drain region being higher than that of the fin; [[and]]
    - a metal gate region formed over to overlap at a top surface and at least one side surface of the fin; and
      - oxide sidewalls formed adjacent to the metal gate region and above the top surface of the fin.
2. (original) The device of claim 1, wherein the metal gate region overlaps the top surface and two side surfaces of the fin.

3. (canceled)

4. (original) The device of claim 1, wherein the source and drain regions are silicided.

5. (original) The device of claim 1, wherein a distance between the insulator and the metal gate region is about 500 Å to about 700 Å and a distance between the insulator and a top of the source or the drain region is about 600 Å to about 1000 Å.

6. (original) The device of claim 1, wherein the metal gate comprises at least one of tungsten, titanium, nickel, TaSiN, and TaN.

Claims 7- 14. (canceled)

15. (original) A FinFET device comprising:  
an insulator;  
a semiconductor layer formed on the insulator, the semiconductor layer including a fin portion corresponding to a channel of the semiconductor device;  
a source region formed from a first end of the semiconductor layer, a height of the source region being higher than that of the fin and a width of the

source region being wider than that of the fin;

a drain region formed from a second end of the semiconductor layer, a height of the drain region being higher than that of the fin and a width of the drain region being wider than that of the fin;

a metal gate region formed to overlap at a top surface and at least one side surface of the fin; and

sidewalls spacers formed adjacent at least portions of the metal gate region.

16. (original) The FinFET device of claim 15, wherein the sidewall spacers have a width ranging from about 150 Å to about 1000 Å.

17. (original) The FinFET of claim 16, wherein the source and drain regions are silicided.

18. (currently amended) The FinFET of claim [[1]] 15, wherein a thickness of the fin portion ranges from about 500 Å to about 700 Å and a thickness of the source and drain regions ranges from about 600 Å to about 1000 Å.

19. (New) The semiconductor device of claim 1, wherein the sidewall

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spacers have a width ranging from about 150 Å to about 1000 Å.